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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 20040324

Application Number: 09/723,655
Filing Date: November 28, 2000
Appellant(s): HERMAN, THOMAS

Kourosh Salehi
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed February 12, 2004.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Invention

The summary of invention contained in the brief is deficient because appellant states "In addition, as a result of a process according to the present invention, the thickness of the spacers is no longer of critical interest in that the spacers are not used to control the size of other features in the device. By eliminating a critical feature, processing is simplified. That is, simply stated, by removing a complexity (critical dimension of the spacers) from the process fewer problems can occur during the processing, thereby increasing yield. An increase in yield improves cost-effectiveness which is of great industrial importance in the competitive field of power

semiconductor processing." There is no discussion of spacers not being used to control the size of features in the device, simplifying the device by removing the spacers, or increasing the yields of the device in the originally filed specification. This discussion seems to be in direct response the to Davies reference. None of these features were discussed in the originally filed specification. Therefore, for at least these reasons, the "**Summary of Invention**" section provided by the appellant attempts to add new matter to the invention disclosed in the originally filed specification.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

Appellant's brief includes a statement that claims 9-14, 21 and 22 do not stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

5,155,052	Davies	10-1992
5,474,946	Ajit et al.	12-1995

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 9 – 14 and 21 – 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Davies (USPAT 5155052, Davies) in view of Ajit et al. (USPAT 5474946, Ajit).

Davies discloses in figures 1 – 4 the process of manufacturing a MOS gated device.

Davies discloses in figures 1 – 4 forming a gate oxide layer (13) atop a silicon surface (11) of one conductivity type. Davies discloses in figures 1 – 4 forming a layer of polysilicon (14) atop the gate oxide layer. Davies discloses in figures 1 – 4 etching the polysilicon layer and the underlying gate oxide layer into a plurality of spaced stripes (left and right 14 and 13) of oxide and polysilicon overlying the silicon surface. Davies discloses in figures 1 – 4 implanting and diffusing a spaced first base diffusion stripe (12) of the other conductivity type into the silicon surface, using the stripes of oxide and polysilicon as a mask. Davies discloses in figures 1 – 4 implanting and diffusing a source diffusion (15) in to the first base diffusion stripes, using the stripes of oxide and polysilicon as a mask, and leaving invertible channel regions (26) along the outer edges of the first base diffusion stripes. Davies discloses in figures 1 – 4 implanting and diffusing second base diffusion stripes (17) into the silicon surface, using the stripes of oxide

and polysilicon as a mask, to a depth below that of the source diffusions and extending to the space between the opposite edges of adjacent pairs of the polysilicon stripes. Davies discloses in figures 1 – 4; and column 4, lines 38 – 43 wherein the stripes of oxide and polysilicon do not include sidewall spacers during implanting and diffusing of the first base diffusion stripes, the source diffusions, and the second base diffusions. Davies teaches in figures 1 – 4 and column 3, lines 29 – 30 that the stripes of oxide and polysilicon are spaced 7.5 – 10.5 microns. It is well known in the art to vary dimensions of device features within the same order of magnitude as a matter of design choice, and Ajit teaches in figure 2 and column 29 – 31 stripes which are spaced apart by a gap of about 3 microns. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the spacing of Ajit in the method of Davies in order to use smaller geometries as photolithography techniques improve as stated by Davies in column 3, lines 27 – 33.

With regard to claim 10, Davies teaches in column 3, lines 27 – 30 wherein the polysilicon stripes have a width of 3.1 microns. The combination of Davies (column 3, lines 27 – 33) and Ajit obviously teach wherein the polysilicon stripes have a width of 1.25 microns in order to use smaller geometries as photolithography techniques improve.

With regard to claims 11 and 12, Davies teaches in column 3, lines 47 – 63 wherein the first base diffusions have a depth of 1.25 microns and the source diffusions have a depth of 0.4 microns.

With regard to claim 13, Davies discloses in figures 1 – 4 formation of insulation spacer layers (18) over the top and edges of the polysilicon stripes and the etching of shallow openings through central portions of the source regions and into the first base diffusions and thereafter

depositing a metal layer (22) over the upper surface of the device to contact the source regions and the first and second base diffusions.

With regard to claim 14, Davies figures 1 – 4 formation of insulation spacer layers (18) over the top and edges of the polysilicon stripes and the etching of shallow openings through central portions of the source regions and into the first base diffusions and thereafter depositing a metal layer (22) over the upper surface of the device to contact the source regions and the first and second base diffusions.

With regard to claim 21, Davies and Ajit further teach that it is obvious wherein the polysilicon stripes are spaced 1.5 microns apart.

With regard to claim 22, Davies and Ajit further teach that it is obvious wherein the polysilicon stripes are spaced 3.2 – 3.4 microns apart.

(11) Response to Argument

With regard to appellant's argument that "Davies does not teach using the oxide and polysilicon stripes in forming the second base diffusions. Indeed, Davies teaches the opposite," it should be noted in figure 2 of Davies that the second base diffusion stripes (17) are formed using the oxide and polysilicon stripes (patterns of 13 and 14, see figure 1 also). It is not clear why appellant states that Davies teaches the opposite, when clearly Davies teaches this feature. Therefore, appellant's arguments are not persuasive, and the rejection is proper.

With regard to the appellant's arguments that "Davies teaches forming sidewall spacers 18 before forming low resistivity regions 17," it should be noted that Davies, in column 4, lines 38 – 43, specifically recites the situation where sidewall spacers are not used in implanting the

low resistivity regions 17 which correspond to the claimed second base diffusion. Thus Davies teaches in figures 1 – 4 and column 4, lines 38 – 43 the limitation wherein the stripes of oxide and polysilicon do not include sidewall spacers during implanting and diffusion of the second base diffusion. Therefore, the arguments are not persuasive, and the rejection is proper.

With regard to the appellant's argument that "Davies actually teaches away from using the oxide and polysilicon stripes as a mask in forming the second base regions (low resistivity regions 17)," it should be noted Davies never states that the claimed situation cannot produce a working device. While Davies suggests in column 4, lines 25 – 43 "it has been found that if a thin oxide, analogous to oxide 15 [which is a misprint and should be 'oxide 16'] shown in FIG. 1, is used rather than a sidewall spacer 18, insufficient separation between base 12 and low resistivity region 17 is provided, and correspondingly low yields result," [emphasis added] it is clear that insufficient separation does not make the device inoperable. Low yields, whether good or bad, do not make Davies teach away from the subject matter. On the contrary, the low yields cited by Davies when sidewall spacers are not used prove that this method is disclosed and does produce a working device. Therefore, appellant's arguments are not persuasive, and the rejection is proper.

With regard to appellant's argument that "It is quite clear that in the example provided by Davies a thin oxide wall (i.e. a thin sidewall) is used in preparing the device," attention is drawn to Davies column 3, lines 36 - 39 "Oxide 16, however, does not materially affect subsequent processing in accordance with the present invention." Also, attention should be drawn to column 4, lines 40 - 41 "oxide 15 shown in FIG. 1, is used rather than a sidewall spacer 18". A quick review of Davies indicates that "oxide 15" in column 4, lines 38 - 43, and "Oxide 16" in column

3, lines 36 - 39, are the same oxide. One of ordinary skill in the art would recognize a sidewall spacer such as element 18 will materially affect subsequent processing. Therefore, a layer that "does not materially affect subsequent processing," and is used "rather than" a sidewall would not be recognized, by one of ordinary skill in the art, to be a "sidewall spacer". Thus, Davies does discloses a situation where sidewall spacers (18) are not used in implanting the low resistivity regions. Therefore, appellant's arguments are not persuasive, and the rejection is proper.

With regard to appellant's argument that "Davies quite clearly says that too thin a sidewall destroys the device. From this statement it is logical to conclude that eliminating the sidewalls destroys the device;" it should be noted that a reference must be considered as a whole. Davies in column 4, lines 35 – 43 explains that "destroying the device" actually refers to the result of "correspondingly low yields" when the sidewall spacer (18) is not used for the second base diffusion (17). Thus, taken as a whole, Davies teaches that some working devices, albeit from a low yielding process, will result when sidewall spacers are not used during the second base diffusion. Therefore, appellant's arguments are not persuasive, and the rejection is proper.

With regard to appellant's argument that "the term low yield teaches away from the invention," it should be noted that a disclosure of a working device produced with no sidewalls present during the second base diffusion cannot teach away from itself. Even though Davies discourages the ordinary artisan from using a process with no sidewalls, nothing in Davies suggests that the process will not produce some working devices when using no sidewalls during the second base diffusion formation. The mere fact that Davies discloses a process using no

sidewalls during the formation of the second base diffusion means that Davies can be used for this feature. Therefore, appellant's arguments are not persuasive, and the rejection is proper.

It can be seen from the disclosure of Davies, the final rejection, and the above, supporting response to appellant's arguments, that Davies fully supports the claimed feature of "said stripes of oxide and polysilicon do not include sidewall spacers during implanting and diffusing of said first base diffusion stripes, said source diffusions, and said second base diffusions." Appellant's arguments that Davies "does not teach using the oxide and polysilicon stripes in forming the second base diffusions," "teaches forming sidewall spacers 18 before forming low resistivity regions 17," "teaches away from using the oxide and polysilicon stripes as a mask in forming the second base regions (low resistivity regions 17)", "thin oxide wall (i.e. a thin sidewall) is used in preparing the device," and "quite clearly says that too thin a sidewall destroys the device," are not supported by the teaching of Davies as explained in the above response. Therefore, appellant's arguments are not persuasive, and the final rejection of Davies in view of Ajit is proper.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Paul E Brock II
March 26, 2004

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